

PRANAB SARMA

pranab.sarma@SCSages.com +1 307 459-1954

IC Package Technology professional with 15+ years track record of delivering cost effective solutions from concept to high volume manufacturing, on time and within budget. I create effective and efficient solutions to challenging problems, influence stakeholders and lead programs and teams to achieve goals.

Passionate about improving products and processes; saving time, improving quality and lowering costs by developing and implementing new products and processes that deliver significant sustainable results. Excellent communication skills and customer focus; succinct problem definition, solution prioritization, execution and follow through.

MS and MBA; technical fluency with financial focus and expertise across the IC Packaging value chain from Product Management to Customers. Strong working experience in cross functional, multi-national and multi-cultural work environments.

AREAS OF EXPERTISE

New Package development and design
Supplier Selection and Qualification
Package reliability and qualification

Technical Program Management/Application Engg.
Product Line Management/Business Development
Cost Reduction and Profitability Management

ACCOMPLISHMENTS

- Led package engineering and qualification activities for stacked die products, BGA and FBGA(CSP), with revenue exceeding \$200M annually; responsible for full range of New Product and New Business Development activities.
- Drove packaging activities from customer design request stage to high volume production release; material selection, qualification and implementation of BOM including mold compound, adhesives and substrates to gain new business revenue of \$40M in 2012.
- Qualified and introduced thin die (75um) and low wire loop for 4 die stacked FBGA(CSP) packages .
- Qualified and introduced first in house PBGA package in AMD to support chipset products.
- Successfully qualified and implemented cost reduction activities including Au wire diameter reduction, thin Au plating and conversion to Cu wire to ensure continuous profitability of product line.

PROFESSIONAL EXPERIENCE

Independent Packaging Consultant

2013 – Present

Providing technical consultancy to fabless semiconductor companies for new product introduction, package development, packaging material selection and qualification including mold compounds, die attach, substrates and leadframes, solder materials and fluxes. Provide business intelligence and analysis to customers regarding supplier selection and development of OSATs.

ASE, Sunnyvale

2011- 2013

Application Engineering / Technical Program Management

- Provided technical support to sales team to support 5 customers. Drove packaging technology solutions to qualify and introduce WLCSP, Flip Chip and aQFN packages. Qualified packaging materials including mold compound, adhesives and substrates to support growth of new products at customers.
- Led technical sales effort including RFQs, material selection, BOM qualification and implementation to gain new business revenue of \$40M in 2012.
- Developed a FlipChip MCM with ASIC logic device, known good memory package and passives for network storage area.

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STATS ChipPAC Inc., Fremont

2003 – 2011

Technical Program Manager

2010 – 2011

- Qualified and introduced WLCSP package solution within three months from package request to low volume manufacturing resulting in new business opportunity of \$1M in first year.
- Qualified and introduced VQFNs-st products with Cu wire bonds to meet time to market deadline.
- Developed, qualified, and started volume manufacturing for QFN, WLCSP, and FlipChip packages.

Product Engineering Manager/Product Line Manager

2003 – 2010

- Led product engineering activities to qualify and introduce stacked die products, BGA and LFBGA with revenue exceeding \$200M annually.
- Developed and introduced thin die (75 um) and low wire loop solution for stacked die wire bond products .
- Drove NPI engineering activities to qualify and introduce packaging materials including mold compounds, adhesives and substrates by working in close collaborations with international suppliers to ensure growth of product lines.
- Implemented material qualification activities with off shore factories for timely introduction of new products.
- Led cost analysis activities and value engineering projects. Successfully qualified and implemented cost reduction activities including Au wire diameter reduction from 1mil to 0.6 mils, thin Au plating from 0.5um to 0.3 um and conversion to Cu wire to ensure continuous profitability of product line.
- Provided technical lead for new package design activities and package characterization.

AMCC (Switching and Network Processing) / MMC Network , Sunnyvale

1999 - 2002

Package Engineering Manager

Drove all phases of IC package design, development and qualification activities including assembly process development, materials, supplier and technology selection and qualification.

- Introduced the first organic FlipChip package at AMCC (SNP) to meet the demand of high performance, high pin count packaging.
- Implemented corporate wise migration to plastic laminate packages from leadframe packages to meet performance requirement. Led packaging activities with cross-functional and global engineering teams of design, test, product, quality and reliability engineers to ensure timely introduction of new packages.
- Saved nearly \$250K of NRE budget in three years by working diligently with suppliers, sub-contractors, and AMCC Supply Management team.

ADVANCED MICRO DEVICES, Sunnyvale

1994 - 1999

Senior Packaging Engineer

Designed, developed and drove package development activities including material, supplier and sub contractor selection and qualification from concept to high volume production for the first in-house laminate BGA chipset package supporting K6 products. Developed a qualification ranking matrix(TCQFS) to shortlist two substrate suppliers from a list of nine international vendors and two sub contractors from a list of six sub contractors.

Computer Skills: MS Office, Autocad., MS Project. Familiar with ANSYS, APD, Flowtherm, JMP.

EDUCATION

M.B.A., San Jose State University

M.S. Engineering (Microelectronics Packaging), San Jose State University